REMARKS

Claims 42 – 48 are pending. Claims 42 – 44 were amended. Claims 1 - 41 were previously cancelled. No new matter has been added. Reconsideration is requested.

Claim 44 was previously amended from depending on claim 43 to depending on claim 42. It has now been amended to recite "The library" and to depend from claim 43.

CLAIM REJECTIONS

Claims 42 – 48 have been rejected under 35 USC 102(a) as being unpatentable by Goren et al. ("An interconnect-aware methodology for analog and mixed signal design, based on high bandwidth (over 40GHz) on-chip transmission line approach").

Applicants respectfully disagree. The authors of Goren et al. include the inventors of the present application with the addition of Israel Wagner and Tiberiu Galambos. Neither Israel nor Tiberiu were inventors of the subject matter on pages 1 – 4 of the publication, which subject matter was cited by the Examiner in the current Office Action. Attached please find a Rule 132 declaration by Israel Wagner and Tiberiu Galambos to that effect.

Thus, Goren et al. is not prior art under 35 USC 102(a) since the subject matter therein that was cited by the Examiner was not "by others", as required by 35 USC 102(a) but, rather, by the present inventors.

Applicants respectfully request the withdrawal of this rejection.

Claim 42 has been rejected under 35 USC 102(a) as being unpatentable by Miller et al. (US 6,539,531).

Miller et al. does not show, *inter alia*, "selecting one of a library of pre-defined transmission line topologies for critical interconnect lines of said integrated circuit." Instead, Miller et al. show a library for interconnect lines between internal and external circuits. This can be seen in the following quotes:

"The present invention relates in general to a process of designing, simulating, fabricating, testing and interconnecting integrated circuits (ICs), and in particular to a method for fully integrating the interconnect systems that are to connect ICs to external circuits into all stages of that process." (Field of Invention)

"Interconnect Systems

As a part of the IC design process, IC designers must concern themselves with the structures that connect nodes of an IC to external circuits. In a typical packaged IC, each circuit node that is to communicate with external circuits is linked to a bond pad on the surface of the IC chip. A bond wire connects the bond pad to a conductive leg extending from the package surrounding the IC chip. When the IC is mounted on a printed circuit board (PCB) the package leg is usually soldered to a PCB trace on the surface of the PCB. When bond pads of one or more other ICs mounted on the PCB are linked to the PCB trace, the bond pads, bond wires, package legs, and the PCB trace form an interconnect system for conveying signals between nodes of two or more ICs. Other interconnect systems are also used. For example, in "solder ball" IC packages the bond wires link the IC pads to balls of solder on the underside of the package that bond to PCB traces when the IC is installed on a PCB." (col. 2, line 53 – col. 3, line 3)

"In high frequency applications an interconnect system can severely attenuate and distort signals passing between the IC and external circuits." (col. 3, lines 52 – 53)

"While IC designers must sometimes be concerned with the frequency response of an entire interconnect system linking a node of an IC to a node of an external circuit, the design tools they work with treat the internal and external components of an interconnect system in a somewhat fragmented manner. Conventional IC cell libraries typically include separate physical and behavioral models of various portions of an IC interconnect system that are internal to the IC such as drivers, receivers, ESD devices, bond pads and the like. However, such cell libraries do not include models of the portions of the interconnect system external to an IC such as bond wires and package legs,

litho-spring or wire-spring contacts, microstrip traces, circuit board vias and the like because they are not part of the IC." (col. 4, lines 10 – 23)

Miller et al. is concerned with a different type of interconnect system, a system which links "a node of an IC to a node of an external circuit" Such an interconnect system is not "for critical interconnect lines of said integrated circuit" as recited in amended claim 42.

Applicants respectfully request the withdrawal of this rejection.

Claims 43, 45 and 46 have been rejected under 35 USC 103(a) as being unpatentable over Miller et al. in view of Chang et al. (US 6,381,730).

Applicants respectfully traverse the rejection because a prima facie case of obviousness has not been established.

The combination of Miller et al. and Chang et al. does not teach or suggest all the limitations of claims 43, 45 and 46. Miller et al. has been discussed above. That discussion is applicable here. It is also noted that claim 43 recites, *inter alia*,

> "a set of transmission line topologies for critical interconnect lines of an integrated circuit capable of carrying analog and mixed signals, which topologies comprise return paths therein"

Miller et al. does not show a library of transmission line topologies "for critical interconnect lines of said integrated circuit" as now recited in amended claim 43.

The addition of Chang et al. does not cure this deficiency. Chang et al. addresses the extraction process, which provides analysis of an existing on-chip interconnect. Chang et al. suggests a way to include inductance computation for every interconnect wire, in addition to resistance and capacitance extraction. For this, Chang et al. considers the current return path, which is necessary to know for inductance computation, as unknown. For each interconnect wire, Chang et al. suggests a very complicated and time consuming process of trying different assumptions about its current return path, which results in a large set of inductance values, from which a "reasonable" value is eventually chosen. This process is based on huge reference

tables built as a preliminary step from field solver runs, "which may number in the tens of thousands for each process" (col. 4, paragraph 60).

The reason that Chang et al. have to perform such difficult calculations is that Chang et al. performs its calculations after the chip is designed.

Miller et al. may provide topologies, but they are for between-node interconnects. Chang et al. does not provide topologies. As a result, Chang et al. does not have return paths therein.

Accordingly, the combination of Miller et al. and Chang et al. does not anticipate claims 43, 45 and 46 and thus, this rejection should be withdrawn.

Claim 44 has been rejected under 35 USC 103(a) as being unpatentable over Miller et al. in view of Suaya et al. (US 2003/0131334).

Applicants respectfully traverse the rejection because a prima facie case of obviousness has not been established.

The combination of Miller et al. and Suaya et al. does not teach or suggest all the limitations of claim 44, now dependent on claim 42. Miller et al. has been discussed above with respect to claim 42. That discussion is applicable here.

Miller et al. show a library for interconnect lines between internal and external circuits. Suaya et al. discuss optimizing on-chip interconnect lines to reduce signal delays on them. The combination of the two does not provide the library recited in claim 43 nor the limitation of dependent claim 44.

Accordingly, Applicants respectfully assert that this rejection should be withdrawn.

Claims 46 and 47 have been rejected under 35 USC 103(a) as being unpatentable over Miller et al. in view of Chang et al. and further in view of Tsividis Y. ("Mixed analog-digital VLSI devices and technology").

Applicants respectfully traverse the rejection because a prima facie case of obviousness has not been established.

The combination of Miller et al., Chang et al. and Tsividis does not teach or suggest all the limitations of claims 46 and 47. The combination of Miller et al. and Chang et al. has been discussed above with respect to claim 43. That discussion is applicable here. The addition of Tsividis does not cure the deficiencies of the combination of Miller et al. and Chang et al. Accordingly, Applicants respectfully assert that this rejection should be withdrawn.

Accordingly, Applicants respectfully assert that amended independent claims 42 and 43 are allowable. Claims 44 - 48 depend from, directly or indirectly, claims 42 and 43, and therefore include all the limitations of those claims. Therefore, Applicants respectfully assert that claims 44 – 48 are likewise allowable. Accordingly, Applicants respectfully request that the Examiner withdraw the rejections to claims 42 – 48.

Applicants believe that the above amendments and remarks are fully responsive to all the objections and grounds of rejections by the Examiner. In view of the foregoing amendments and remarks, the Applicants respectfully submit that all the pending claims are deemed to be allowable. Their favorable reconsideration and allowance is respectfully requested.

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

Please charge any fees associated with this paper to deposit account No. 09-0468.

Respectfully submitted,

Date: October 9, 2006

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